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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 8 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

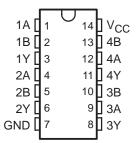
The 'LV86A devices are quadruple 2-input exclusive-OR gates designed for 2-V to 5.5-V $\rm V_{CC}$ operation.

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function

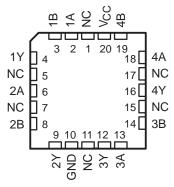
 $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

SN54LV86A . . . J OR W PACKAGE SN74LV86A . . . D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



SN54LV86A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

TA	PACK	AGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	0010 D	Tube of 50	SN74LV86AD	11/004
	SOIC - D	Reel of 2500	SN74LV86ADR	LV86A
	SOP - NS	Reel of 2000	SN74LV86ANSR	74LV86A
-40°C to 85°C	SSOP – DB	Reel of 2000 SN74LV86ADBR		LV86A
		Tube of 90	SN74LV86APW	
	TSSOP – PW	Reel of 2000	SN74LV86APWR	LV86A
		Reel of 250	SN74LV86APWT	
	TVSOP - DGV	Reel of 2000	SN74LV86ADGVR	LV86A
	CDIP – J	Tube of 25	SNJ54LV86AJ	SNJ54LV86AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54LV86AW	SNJ54LV86AW
	LCCC - FK	Tube of 55	SNJ54LV86AFK	SNJ54LV86AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

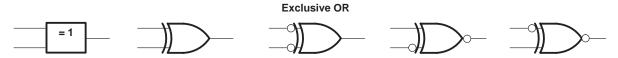


FUNCTION TABLE (each gate)

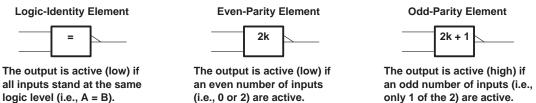
INP	UTS	OUTPUT
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'LV86A gate in positive logic; negation can be shown at any two ports.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high-	-impedance	
or power-off state, VO (see Note 1)		–0.5 V to 7 V
Output voltage range, VO (see Notes 1 and 2)		$0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–20 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±25 mA
Continuous current through V _{CC} or GND		±50 mA
Package thermal impedance, θ _{JA} (see Note 3):	D package	86°C/W
	DB package	96°C/W
	DGV package	127°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 5.5 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 4)

			SN54	LV86A	SN74I	_V86A	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2	5.5	2	5.5	V
		V _{CC} = 2 V	1.5		1.5		
V	High level input valtage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V _{CC} × 0.7		$V_{CC} \times 0.7$		V
VIH	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V _{CC} = 2 V		0.5		0.5	
l ,,	Law layel input valtage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	V
VIL	Low-level input voltage	V _{CC} = 3 V to 3.6 V		V _{CC} ×0.3		$V_{CC} \times 0.3$	V
		V _{CC} = 4.5 V to 5.5 V		V _{CC} ×0.3		$V_{CC} \times 0.3$	
٧ı	Input voltage		0	5.5	0	5.5	V
VO	Output voltage		0	Vcc	0	VCC	V
		V _{CC} = 2 V	3	-50		-50	μΑ
	Liber level evident evident	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	90	-2		-2	
ЮН	High-level output current	V _{CC} = 3 V to 3.6 V	Q	-6		-6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12		-12	
		$V_{CC} = 2 V$		50		50	μΑ
	Law layed autout aumant	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2		2	
lOL	Low-level output current	V _{CC} = 3 V to 3.6 V		6		6	mA
		V _{CC} = 4.5 V to 5.5 V		12		12	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200		200	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3 V \text{ to } 3.6 V$		100		100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20		20	
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		.,	SN5	4LV86A		SN7	4LV86A			
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1				
V	I _{OH} = -2 mA	2.3 V	2			2			V	
Voн	I _{OH} = -6 mA	3 V	2.48	, S		2.48			V	
	I _{OH} = -12 mA	4.5 V	3.8	, N		3.8				
	I _{OL} = 50 μA	2 V to 5.5 V		PA	0.1			0.1	0.4 V	
	I _{OL} = 2 mA	2.3 V	į		0.4			0.4		
V _{OL}	I _{OL} = 6 mA	3 V	2		0.44			0.44		
	I _{OL} = 12 mA	4.5 V	70%		0.55			0.55		
lį	V _I = 5.5 V or GND	0 to 5.5 V	Q		±1			±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			20	μΑ	
l _{off}	V_{I} or $V_{O} = 0$ to 5.5 V	0			5			5	μΑ	
Ci	$V_I = V_{CC}$ or GND	3.3 V		1.4			1.4		pF	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	LOAD	T _A = 25°C		SN54LV86A	SN74LV86A			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
t _{pd}	A or B	Υ	C _L = 15 pF		7.9*	17.6*	1* 21*	1	21	ns
t _{pd}	A or B	Y	C _L = 50 pF		10.5	22.6	1 26.5	1	26.5	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

FROM T		то	TO LOAD	T _A = 25°C		SN54LV86A	SN74LV86A			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
t _{pd}	A or B	Υ	C _L = 15 pF		5.5*	11*	1* 13*	1	13	ns
t _{pd}	A or B	Υ	C _L = 50 pF		7.4	14.5	1 16.5	1	16.5	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

FROM TO		то	LOAD	T _A = 25°C		SN54LV86A		SN74LV86A			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN M	AX	MIN	MAX	UNIT
t _{pd}	A or B	Υ	C _L = 15 pF		3.7*	6.8*	13/11/2	8*	1	8	ns
t _{pd}	A or B	Υ	C _L = 50 pF		5.3	8.8	Q1	10	1	10	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

SN54LV86A, SN74LV86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

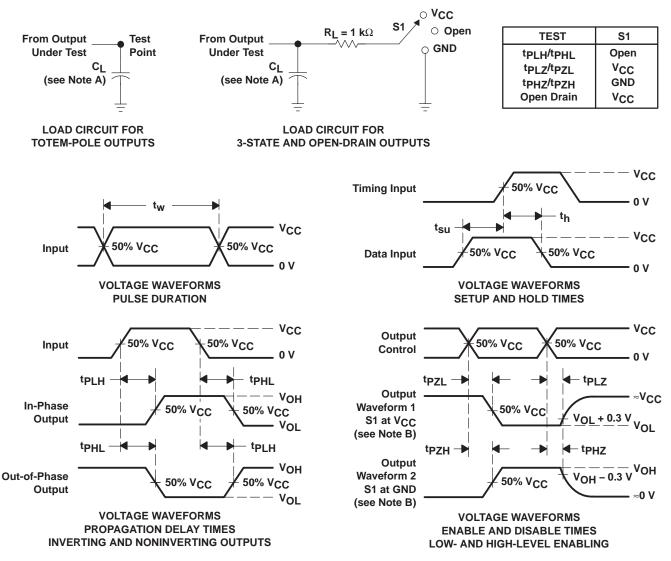
	DADAMETED	SN	LINUT		
	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.2	8.0	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.1	-0.8	V
VOH(V)	Quiet output, minimum dynamic VOH		3.1		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CO	VCC	TYP	UNIT	
<u> </u>	Dower discination conscitones	C. F0 nF	f 40 MH I-	3.3 V	8.4	~F
Cpd	Power dissipation capacitance	$C_L = 50 \text{ pF},$	f = 10 MHz	5 V	8.8	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \le 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f \le 3 \text{ ns}$, $t_f \le 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpz and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV86AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV86APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs. **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



PACKAGE OPTION ADDENDUM

18-Sep-2008

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LV86A:

Automotive: SN74LV86A-Q1

Enhanced Product: SN74LV86A-EP

NOTE: Qualified Version Definitions:

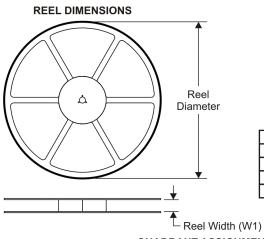
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications





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TAPE AND REEL INFORMATION

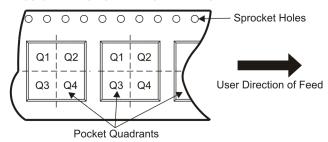




	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

- Reel Width (W1)

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV86ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV86ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV86ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV86ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV86APWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV86ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LV86ADGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74LV86ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LV86ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LV86APWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.



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